IN THE CLAIMS

Claims 4-6, 9 and 13-14 are pending in this application. Please cancel claims 1-3, 7-8, 10-12 and 15-22 without prejudice or disclaimer, amend claims 4, 9 and 13, as follows:

1-3. (Canceled)

4. (Currently Amended) A semiconductor integrated circuit device ~~according to claim 1~~ , comprising: an input terminal for receiving an input signal including any one of an instruction, a data, a position where the data exists, or a timing signal; and

an output terminal for producing a signal formed by an internal circuit in response to the input signal or a signal fed through the input terminal, wherein the instruction, the data, the position where the data exists and the timing signal output from the output terminal are those that have been re-adjusted by a timing signal reproduced therein.

5. (Original) A semiconductor integrated circuit device according to claim 4, wherein the timing signal that is re-adjusted is the one formed by a phase synchronizing loop circuit that receives a reference timing signal.

6. (Original) A semiconductor integrated circuit device according to claim 5, wherein the reference timing signal is the one input from an external unit.

7-8. (Canceled)

9. (Currently Amended) A memory system ~~according to claim 8~~, comprising:

a plurality of semiconductor integrated circuit devices each having an input terminal for receiving an input signal containing any one of an instruction, a data, a position where the data exists or a timing signal, and an output terminal for producing a signal formed in an internal circuit in response to the input signal or fed through the input terminal; and

a signal-forming circuit for forming an input signal containing any one of the instruction, the data, the position where the data exists or the timing signal for the semiconductor integrated circuit devices, wherein

the output terminal of the semiconductor integrated circuit device in the preceding stage and the corresponding input terminal of the semiconductor integrated circuit device of the next stage are connected in cascade,

the input signal containing any one of the instruction, the data, the position where the data exists or the timing signal formed by the signal-forming circuit is fed to the input terminal of the semiconductor integrated circuit device of the initial stage in the cascade connection, and

among the signals from the output terminal of the semiconductor integrated circuit device of the final stage in the cascade connection, at least the signal corresponding to the data is transmitted to the signal-processing circuit,

wherein the instruction is a command for specifying the state of operation, the data is the one to be stored; the position where the data exists is an address signal, the timing signal is a clock, and each of the plurality of semiconductor integrated circuit devices includes a memory circuit that operates in response to a command and an address signal input in synchronism with the clock, and

wherein the command, the data, the address and the timing signal output from the output terminal are those that have been re-adjusted by a timing signal reproduced therein.

10-12. (Canceled)

13. (Currently Amended) A memory system ~~according to claim 12~~, comprising: a plurality of semiconductor memory devices each having an input terminal for receiving an input signal containing any one of a command, a data, an address or a timing signal; and an output terminal for producing a signal corresponding to the input signal fed through the input terminal, wherein among the plurality of semiconductor memory devices, the output terminal of the semiconductor memory device in the preceding stage and the corresponding input terminal of the semiconductor memory device of the next stage are connected in cascade,

wherein the input terminal of the semiconductor memory device of the initial stage in cascade receives the command, the data, the address or the timing signal formed by the signal-forming circuit, and, among the output signals produced from the output terminal of the semiconductor memory device in the final stage in cascade, at least a signal corresponding to the data is transmitted to the signal-forming circuit,

wherein the signal-forming circuit is a memory control device constituted by a semiconductor integrated circuit device, and

wherein the command, the data, the address and the timing signal produced from the output terminal are those that are re-adjusted by a timing signal reproduced therein.

14. (Original) A memory system according to claim 13, wherein the timing signal that is re-adjusted is the one formed by a phase synchronizing loop circuit that receives a reference timing signal.

15-22. (Canceled)